CIRCUIT FOR CORRECTION OF DIFFERENTIAL

SIGNAL PATH DELAYS IN A PLL

Field of the Invention

5   The present invention relates to a method and/or architecture for correction of differential signal path delays generally and, more particularly, to a method and/or architecture for correction of skew between an input and an output of a phase locked loop (PLL).

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Background of the Invention

          Referring to FIG. 1, a block diagram of a circuit 10 illustrating a conventional phase locked loop circuit is shown. The circuit 10 includes a multiplexer 12, a number of dividers 14a

15   and 14b and a phase lock loop (PLL) 16. Two or more inputs (i.e., paths IN1, IN2 and IN3) are presented to the multiplexer 12. One input is selected and presented as a reference signal REF, through the divider 14a, to the PLL 16. Another input is selected and presented as a feedback signal FB, through the divider 14b, to the

20   PLL 16. Any one of the inputs (IN1, IN2, or IN3) could be

implemented as the feedback signal FB or the reference signal REF.

A second feedback signal or reference signal can be implemented

from the input IN1, IN2, or IN3. The multiplexer 12 selects the

desired input(s) to be used for the reference and feedback input

5   paths to the PLL 16. The dividers 14a and 14b are implemented as

digital counters or dividers before the PLL 16 to provide for

frequency scaling of the reference and feedback signals. In some

cases, the divider(s) 14a and/or 14b and the multiplexer 12 are not

used.

10   The circuit 10 provides a PLL output frequency FOUT that

is frequency and phase locked to the input reference signal REF.

The frequency FOUT is determined by the integer ratio of the

feedback to reference dividers 14a and 14b. Ideally the phase of

whichever input is selected as the reference signal REF is equal to

15   the phase of the input selected as the feedback signal FB. Phase

error is determined from the difference in arrival times (skew) of

either the rising or falling edge of the reference input REF

relative to the feedback input FB.

Phase can be expressed in radians by dividing the skew by

20   the period and multiplying by 2π (for radians) or 360° (for

degrees). The term "skew" typically implies the long term or

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"average" time difference between signals. The terms "phase noise"

or "jitter" are used to describe the dynamic variations in the

arrival time between signals.

Disadvantages with the circuit 10 include (i) time delay

5   differences through the dividers 14a and 14b and (ii) PLL 16 input

skew errors. Such disadvantages contribute to input skew of the

reference and feedback paths (i.e., skew does not equal zero). For

example, a PLL typically uses an analog charge pump as part of the

phase detection circuit. Analog mismatches cause skew at an input

10   of the PLL to be non-zero. Time delay differences between the

reference and feedback paths show up as non-zero phase skew at the

PLL input as well. Furthermore, delay mismatches in the reference

and feedback paths through the multiplexer 12 also cause phase

skew. Mismatch within the long chain of required digital and

15   analog circuitry for the reference and feedback paths (from the

inputs IN1, IN2, IN3 to the charge pump in the PLL 16) is likely to

cause input skew. Conventional analog charge pumps have one or

more limitations such as P/N current mismatches and differences in

charge injection.

20   Another conventional approach for correction of signal

path delays in PLLs is to implement bang-bang digital control

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loops. Such control loops can be accurate, but are very slow. Conventional bang-bang control loops have a speed/jitter trade-off and can still have skew problems due to charge pump imbalance. Neither of these conventional techniques address time delays in

5   counters and digital circuitry that occur before the PLL.

Summary of the Invention

The present invention concerns an apparatus comprising a first circuit and a second circuit. The first circuit may be

10   configured to (i) select one of a plurality of input signals and (ii) generate (a) an output signal having a frequency and (b) one or more control signals in response to a skew signal. The second circuit may be configured to generate the skew signal in response to the one or more control signals. The first circuit may be

15   configured to minimize skew between the selected input signal and a feedback of the output signal, in response to the skew signal.

The objects, features and advantages of the present invention include providing a method and/or architecture for correction of skew, or time differential, between an input and an

20   output of a phase locked loop (PLL) that may (i) implement digitally based skew, (ii) implement a low frequency phase noise

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reduction circuit, (iii) be applied externally to an existing PLL, (iv) be implemented without changes to the PLL design, (v) be setup with multiple phase comparators to monitor different combinations of inputs, and/or (vi) allow a simple self test of the internal

5   skew of the PLL path.

Brief Description of the Drawings

These and other objects, features and advantages of the present invention will be apparent from the following detailed

10   description and the appended claims and drawings in which:

FIG. 1 is a block diagram of a conventional circuit for differential signal path correction;

FIG. 2 is a block diagram of a preferred embodiment of the present invention;

15   FIG. 3 is a detailed block diagram of the circuit of FIG. 2; and

FIG. 4 is a detailed block diagram of an alternate embodiment of the present invention.

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Detailed Description of the Preferred Embodiments

Referring to FIG. 2, a block diagram of a circuit 100 is shown in accordance with a preferred embodiment of the present invention. The circuit 100 may provide a precision digital phase comparator (to be discussed in connection with FIG. 3) to minimize timing skew in two matched digital clock paths. The circuit 100 may de-skew an input path and PLL in a zero delay buffer.

The circuit 100 generally comprises a block (or circuit) 102 and a block (or circuit) 104. The circuit 102 may be implemented as an output logic circuit that may include a Phase Locked Loop (PLL) to be described in more detail in connection with FIG. 3. The circuit 104 may be implemented as a counter logic circuit. The circuit 102 may have an input 110 that may receive one or more input signals (e.g., IN[1:n], where n is an integer). The particular number of input signals may be varied to meet the design criteria of a particular implementation. The circuit 102 may also have an output 112 that may present one or more signals to an input 114 of the counter logic 104, an input 116 that may receive an indication signal (e.g., SKEW[N:1]) from an output 118 of the counter logic 104, and an output 120 that may present a signal (e.g., FOUT). The signal FOUT may be a periodic signal

oscillating at a particular frequency or a non-periodic signal having a number of edges that are not equally spaced.

The circuit 100 may reduce the skew, or time differential, between a selected one of the input signals IN[1:n] and a feedback of the output signal FOUT. The feedback of the output signal FOUT is generally presented as one of the input signals IN[1:n]. The circuit 100 may also reduce low frequency phase noise of a phase locked loop. In one example, the circuit 100 may be implemented as a skew correction circuit. In another example, the circuit 100 may be implemented as a zero delay buffer. However, the circuit 100 may be implemented for other applications to match two path delays (e.g., the circuit 100 is not necessarily limited to PLL applications).

Referring to FIG. 3, a more detailed diagram of the circuit 100 is shown. The circuit 102 generally comprises a comparator block (or circuit) 130, a multiplexer block (or circuit) 132, a counter 134, a counter 136, a delay block (or circuit) 138, a phase lock loop circuit 140 and a buffer 142. The delay circuit 138 may be implemented as a digitally programmable delay line circuit. In another example, the delay circuit 138 may be implemented as a skew generation circuit. The comparator section

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130 may be implemented as a number of comparators 150a-150n. The circuit 104 generally comprises a multiplexer 160 and a counter 162. One of the signals IN1, IN2, IN3 may be implemented as a reference signal presented to the counter 134. One of the signals

5   IN1, IN2, IN3 may be implemented as a feedback signal presented to the counter 136.

Referring to FIG. 4, an alternate embodiment of a circuit 100' is shown. The circuit 100' may be similar to the circuit 100. The circuit 100' may illustrate digital detection/correction within

10   the PLL 140'. The precision digital phase comparator 130' may detect phase differences between the signal REFIN and the signal FB. The frequency of the signal FB may be a high frequency (e.g., 400 MHz or more). In such an example, the counter 136' may be implemented as a 1/4 frequency counter and may integrate phase

15   error. The delay correction circuit 138' may compensate for skew in response to the signal SKEW(N:1) received from the counter 162'. Additionally, the circuit 100' may have multiple input paths (e.g., greater than one reference clock signal and greater than one feedback clock signal). The delay correction circuit 138' may be

20   a digitally programmable analog delay.

The precision phase comparator block 130' (or 150a-150n of FIG. 3) generally produces a digital "1" or a digital "0" output, depending on whether reference signal REFIN is leading or lagging in time compared with the feedback signal FB. The counters

5   134 and 136 may be implemented as a form of up/down counters that generally integrate the pulses out of the PD block 130. The delay circuit 138 may independently generate a delay difference or skew, between the reference and feedback paths, where the difference is proportional to the digital word SKEW[N:1].

10   Consider the example where the PLL 140 obtains lock and reduces the phase skew to some value based on the above mentioned imperfections. One of the phase detectors 150a-150n is generally chosen (while the other phase detectors 150a-150n are disabled) based on which two of the inputs IN1, IN2, or IN3 is selected. The

15   multiplexer 160 may select the output of the selected phase detector 150a-150n and multiplex the output to the U/D counter 162. If the reference input signal REFIN arrives earlier in phase (time) than the feedback input, then the output of the selected phase detectors 150a-150n is a digital "1". The output of the phase

20   detectors 150a-150n is a digital "0" if the feedback input arrivers earlier.

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When a "1" is presented by a particular phase detector 150a-150n, the U/D counter 162 generally increments an internal count value. If a "0" is presented by a particular PD 150a-150n, the U/D counter 162 generally decrements the internal value. When the counter value increases, the delay circuit 138 may decrease the delay in the reference path REFDLY while increasing the delay in the feedback path FBDLY.

Consider the example where the PLL 140 has converged such that the reference signal REFIN is leading in phase compared to the feedback signal FB. The reference counter 134 and multiplexers 132 may have more time delay than the feedback counter 136. Thus, the reference signal REFIN needs to arrive earlier than the feedback signal FB. However, the condition may also be due to an imbalance in the analog charge pump currents (e.g., within the PLL 140).

If the delay difference (or skew) is great enough, the phase detector 130 will generate all 1's. If the skew is less than the jitter in the circuit 100, the phase detector circuit 130 will generate 1's and 0's but on average will generate more 1's. As a result, the counter value of the U/D counter 162 will increase over time. As the counter value increases, delay is removed from the reference path REFDLY and added to the feedback path FBDLY. The

counter value continues to increase until on average as many 1's

come out of the PD circuit 130 as 0's. Thus, the average skew at

the input may be minimized to within the accuracy of the phase

detector circuit 130.

5   In this manner, the circuit 100 may remove the static

skew and may also remove time varying skew as well. The amount of

attenuation of time varying skew is dependent on the frequency of

the time variations. The circuit 100 may reduce low frequency

phase noise created by the PLL 140.

10   The circuit 100 may be extended to any integer number of

inputs. For higher number of inputs, more comparators may be used

(e.g., N inputs may use N(N-1)/2 comparators). However, for a

basic implementation, the circuit 100 may implement two inputs.

Alternatively, additional multiplexers may be implemented to select

15   relevant inputs. However, multiplexers should be minimized since

they may introduce additional skew.

The phase comparator circuit 130, the skew delay circuit

138 and the U/D counter 162 may have many potential

implementations. The phase comparator circuit 130 may be

20   implemented as a single (or number of) "D" type flip-flops.

Ideally the phase comparator circuit 130 may have zero set-up time,

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since any setup time requirement generates skew at the input. Design considerations may be needed for the circuit 100 if the reference and feedback paths are not running at the same frequency. Different frequencies may be typical in frequency multiplication applications where the feedback is N times the reference frequency. A phase comparison may only be meaningful if made at a transition of the slower running signal. If the phase comparator circuit 130 behaves like a "D" flip-flop, the clock input is generally from the slower running signal such that the output of the flip-flops only changes on the slower signal.

If the application is such that either the reference path or the feedback path may be the higher frequency under different configurations, two-phase comparators for each pair of inputs may be necessary. Such a condition may occur when the system clock is the reference signal and another clock is the feedback signal. A multiplexer may be implemented to select the appropriate comparator output to use. Additionally, comparator designs that accomplish such a task with a single comparator integrated circuit with two output paths may be implemented.

The U/D counter 162 may have a number of special features. One such special feature may be the concept of

"pre-scaling". Pre-scaling may force the counter 162 to count multiple times before changing the digital output. The pre-scaling may be equivalent to dividing the digital output word SKEW[N:1] by a constant before proceeding to the skew delay circuit 138. It may

5   also be desirable to prevent the counter 162 from over-flowing or "wrapping" if the count hits full scale. For example, the counter 162 may be implemented that senses an alternating "1" or "0", ignoring the alternating since the net effect on the final count is zero.

10   The counter 162 may be implemented to update the output whenever the sum changes. Other implementations may only update the final skew output at a certain, fixed times. Various other filtering or counting techniques may be applied to the counter 162. The counter 162 may be a digital filter that integrates the phase

15   detector outputs. Other filters (e.g., linear, non-linear or higher order) may be developed and applied that may have subtle effects on the way the corrections get updated. The discrete switching of skew delay block 138 may add noise to the loop. The spectrum of the noise may be controlled to some extent by

20   performing filtering with the counter 162. Appropriate

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implementations of the U/D counter 162 may drive the average skew to zero.

Digital signals may also be added to the counter 102 to add desired skew or dynamic phase changes to the output signal

5   FOUT. For example, the output signal FOUT may be phase modulated by adding a time varying digital phase offset to the counter output SKEW[N:1].

The circuit 100 may be implemented with basic self test capability. The design of the circuit 100 may be varied to provide

10   ability to read or set the counter values from an external source. The configurable counter values may allow the circuit 100 to implement self-test features. For example, the skew delay 138 performance may be measured by adjusting the counter values and observing the change in skew. Test modes may also be implemented

15   to by-pass the PLL 140 and measure time delay changes through the circuit 100. By reading the counter values after the loop has converged, a basic measurement of skew for the internal parts (e.g., the multiplexers 132, counters 134, 136 and PLL 140) may be obtained. If the skew on the internal parts is larger than

20   expected the circuit 100 may be discarded as marginal. By allowing the circuit 100 to "converge" and then read the contents of the

counter 102, the built in skew of the part that is being corrected

may be determined.

The programmable skew delay block 138 may be implemented

in a number of ways. In one implementation, the reference path

5   delay REFDLY may decrease while the feedback path delay FBDLY may

increase. One path may have a fixed delay, while the other delay

path changes (or a combination of both of the delay paths). The

reference delay REFDLY may change for one part of the range, while

the feedback delay path changes. In general, the skew delay

10   circuit 138 may be implemented such that the changes in delay are

small enough not to cause appreciable additional jitter at the

output of the PLL 140.

The circuit 100 may (i) correct digital timing skew, (ii)

provide a PLL with the addition a digital skew correction circuit,

15   (iii) be capable of self testing skew of a PLL circuit, (iv)

correct the skew of multiple digital inputs to a PLL, (v) correct

the skew of a PLL completely external to the PLL, and/or (vi)

reduce the low frequency phase noise of a PLL (e.g., the circuit

100 may prove matching within 50 pS (< 100 pS)).

20   The circuit 100 may achieve low skew and low frequency

phase noise. Low skew and frequency phase noise may be provided by

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the comparator circuit 130, the counter 162 and the delay block

138. The phase detector 130 may be simple and precise. The phase

comparator block 130 may become the reference for low frequency and

DC skew errors in the system 100, as opposed to the noisier and

5   less accurate phase detector in the analog PLL 140 and associated

digital circuitry before the PLL 140. A digital, or binary output,

phase   comparator   may   be   more   accurate   than   the   phase

detector/analog charge pump in a PLL. The circuit 100 may remove

path delay differences in digital logic before the PLL 140. The

10   circuit 100 may provide a digitally based skew and low frequency

phase noise reduction circuit. The circuit 100 may be applied

externally to an existing PLL and does not require changes to the

existing PLL. However, the circuit 100 may be implemented along

with a PLL on a single integrated circuit. The circuit 100 may be

15   setup with multiple phase comparators to monitor different

combinations of inputs. The circuit 100 may allow a simple self

test of the internal skew of the PLL path.

The   various   signals   of   the   present   invention   are

generally "on" (e.g., a digital HIGH, or 1) or "off" (e.g., a

20   digital LOW, or 0). However, the particular polarities of the on

(e.g., asserted) and off (e.g., de-asserted) states of the signals

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may be adjusted (e.g., reversed) accordingly to meet the design

criteria of a particular implementation.

  While the invention has been particularly shown and

described with reference to the preferred embodiments thereof, it

5 will be understood by those skilled in the art that various changes

in form and details may be made without departing from the spirit

and scope of the invention.